EXHIBIT J

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; and MICRON TECHNOLOGY TEXAS LLC,
Petitioners,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2022-00236
U.S. Patent No. 9,824,035

PETITIONERS' REPLY

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I. Introduction

Patent Owner Netlist mischaracterizes the claims, the prior art, and the Petition ("Pet.") in its Response. *See* Paper 21 ("Resp."). Based on a full record, the Board should maintain its favorable finding from the Institution Decision, (Paper 16, "Dec."), and determine that the challenged claims are unpatentable.

II. The Challenged Claims Are Rendered Obvious by Osanai and Tokuhiro

Contrary to Netlist's arguments, Ground 1 renders obvious the claimed "*second memory operation*" and "*logic*." The Petition also shows why a person having ordinary skill ("POSITA") would combine Osanai and Tokuhiro. As explained below, Ground 1 shows that the challenged claims are obvious and Netlist's arguments are wrong.

A. Osanai and Tokuhiro Render Obvious a "Second Memory Operation"

Claim 1 recites "*logic. . . configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation*." The Petition mapped Osanai's data register control circuit 320—which includes read and write leveling circuitries—as the claimed "*logic*." Pet. 31–36, 39, 41; Ex. 1005, [0096]. These leveling circuitries perform read and write leveling operations, which set timing information "*based on one or more signals received by the each respective buffer*." Pet. 31–36. The Petition also explained that Tokuhiro discloses a leveling technique

where delay time for a read operation is determined based on another delay time determined by the write leveling operation. *See* Pet. 36–38. The Petition further explained that claim 1 is rendered obvious when Tokuhiro's leveling technique is incorporated by Osanai's read and write leveling circuitries. *See id.*, 38–41. The proposed combination maps the read operation and write leveling operation to the claimed "*first*" and "*second memory operation*," respectively. *See id.* 36–41. Central to the parties' dispute, the Board's institution decision correctly raised "whether the write leveling operation itself teaches the recited 'second memory operation'. . . ." Dec. at 26. As shown below, the evidence confirms that a "write leveling operation" is a "*memory operation*."

The '035 patent describes that "*memory operations*" include other memory operations beyond regular write and read operations. Ex. 1001, 3:27–32 ("[T]he memory module is operable to perform memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.)."). Other memory operations include, for example, those in response to "refresh" and "precharge" memory commands. *Id*. Accordingly, the '035 patent describes that the claimed "*memory operations*" encompass various operations performed by memory in response to memory commands.

Osanai's memory devices perform leveling operations in response to memory commands. Specifically, memory devices perform "leveling operations" in response

to Mode Register Set ("MRS") commands. While a MRS command is not a "*memory operation*" by itself, MRS commands trigger memory operations like write leveling. Ex. 1005, [0146]–[0147]; *see also* Ex. 2013 at 13 ("Memory controller initiates Leveling mode of all [memory] by setting bit 7 of MR1 to 1"). Netlist admits as much. *See* Resp. 24 ("Mode Register Set ('MRS') commands [are] used to enter and exit Write Leveling Mode."). Osanai's memory devices thus receive MRS memory commands to perform leveling operations, which is consistent with the '035 patent's description of "*memory operations*." *See* Ex. 1001, 3:27–32.

Other evidence confirms that leveling operations are "*memory operations*." Both Osanai and Tokuhiro refer to read and write leveling as operations. *See* Ex. 1005, [0096]; Ex. 1006, 1:34–38. Likewise, Netlist's exhibit includes "write leveling" in the subsection titled "DDR3 SDRAM [i.e., Memory] Command Description and Operation." *See* Ex. 2013 at 12; Ex. 1022, 16:22–17:4 (admitting Ex. 2013 is "one source of information that a POSITA" would use "to understand terminology" in the '035 patent). That same exhibit also confirms that Mode Register Set is a memory command included in a table, Ex. 2013 at 8, that includes "read, write, refresh, [and] precharge" commands for "*memory operations*" described in the '035 patent. Ex. 1001, 3:27–32. This table confirms that leveling operations use memory commands like every other "*memory operations*" described

see Ex. 1005, [0146], and its expert's admissions about how Osanai's read leveling works, described above. Ex. 2010, ¶¶ 104–105; *see id.*, ¶¶ 32, 34; Ex. 1022, 70:10–22. Netlist's references to Dr. Alpert's deposition do not help its arguments because they are predicated on Netlist's mischaracterization what the Petition identified as "*data paths*." *See* Resp. 35.

Therefore, Osanai and Tokuhiro render obvious the claimed "*logic*."

C. A POSITA Would Have Modified Osanai's Leveling Circuitries to Incorporate Tokuhiro's Leveling Technique.

Osanai discloses read and write leveling circuitries. *See* Pet. 33–38. Tokuhiro likewise discloses a leveling technique. *See id*. The Petition provides three rationales why a POSITA would have been motivated to incorporate Tokuhiro's leveling technique in Osanai's data register control circuit, which already includes read and write leveling circuitry. Pet. 38–41. Netlist challenges each reason and argues that a POSITA would not combine the references. But those arguments are wrong.

1. Reducing the Number of Steps to Determine a Read Delay

First, the Petition explained that modifying Osanai's data register control circuit would reduce the number of steps needed to determine the read delay by basing that determination on timing information determined during write leveling. Pet. 39 *citing* Ex. 1003, ¶ 126. Dr. Alpert explained that Tokuhiro's leveling technique uses timing information determined for write operations to determine a delay for subsequent read operations. Pet. 38 *citing* Ex. 1003, ¶¶ 121–122; Ex. 1006,

3:16-26, 16:1–28. Tokuhiro explains that "because the wirings for connections between the memory controller 12 and the DIMM 11 are formed in the same length," a mathematical relationship exists between the first delay for write and the second delay for read operations. Ex. 1006, 16:1–28. Tokuhiro describes that the simplification of this mathematical relationship allows for "the second delay time Dt2 [for read operations] [to] be calculated by using the first delay time Dt1 [for write operations] that has been set in the write leveling." Ex. 1006, 16:19–23. Dr. Alpert explained that a POSITA would have recognized that Tokuhiro's mathematical simplification beneficially reduces the number of steps needed by determining the delay timing for read operations using timing information already determined during write leveling. Pet. 39 *citing* Ex. 1003, ¶ 126. Without Tokuhiro's simplification, a memory module would need to make additional measurements or calculations to determine a delay for read operations.

Netlist raises two counterarguments—neither is correct. First, Netlist argues that Tokuhiro does not set a read delay. Tokuhiro's technique "delay[s], in the read operation, a data signal input from the memory by a second delay time that is set based on the first delay time." Ex. 1006, 3:24-26. These delays compensate for a "signal arrival time in read operations," which "are not provided with the JEDEC standard," Ex. 1006, 2:54-59—that is, the problem Tokuhiro's technique solves, *see* Ex. 1006, 2:60–13. This mirrors how Tokuhiro describes write leveling, *see* Ex.

1006, 2:39–49, except that it is for read operations. Tokuhiro thus describes read leveling that determines a delay timing used for read operations.

Second, Netlist attacks whether the proposed combination would achieve the same efficiency. Resp. 43. But, as explained above, modifying Osanai's leveling circuitries would reduce the number of steps needed to determine delay timing for a read operation based on a mathematical relationship exploited by Tokuhiro's write leveling technique. Pet. 39 *citing* Ex. 1003, ¶ 126.

2. Increasing Efficiency

The Petition next explains that a POSITA would have combined Osanai and Tokuhiro based on an express teaching found in Tokuhiro. Pet. 40 *citing* Ex. 1006, 24:26–29, Ex. 1003, ¶ 127. By incorporating Tokuhiro's leveling technique, the Petition explained that Osanai's data register buffer would "efficiently set" the delay times "without increasing power consumption and circuit area." Ex. 1006, 24:26–29. Relying on Dr. Alpert's testimony, the Petition explained that a POSITA would have recognized that the delay calculated using Tokuhiro's leveling technique would be more efficient than conventional read/write leveling techniques that did not account for a write operation's delay. Pet. 40 *citing* Ex. 1003, ¶ 127, Ex. 1006, Figs. 16–17, 21:15–24:42. This efficiency would have motivated a POSITA to incorporate Tokuhiro's technique in Osanai's data register control circuit 320. Pet. 40; Ex. 1003, ¶ 127.

D. Ground 3 Renders the Challenged Claims Obvious

Ground 2 relied on a POSITA's knowledge to render two claimed features obvious. *See* Pet. 61–62, 68–69. Relying on Osanai's teachings, Ground 3 addresses any Netlist arguments that a POSITA would not have such knowledge. *See* Pet. 70–71. Ground 3 relied on Ground 2's reasoning for why a POSITA would modify Takefman. *See* Pet. 70–71. Without Netlist contesting that these features are outside a POSITA's knowledge, Grounds 2 and 3 show the challenged claims are obvious over Takefman and Tokuhiro, with or without Osanai.

IV. Conclusion

For the foregoing reasons and those in the Petition, the challenged claims are unpatentable.

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Respectfully submitted,

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